

Performance Evaluation and Comparison of Ultra-thin Bulk (UTB), Partially Depleted and Fully Depleted SOI MOSFET using Silvaco TCAD Tool

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Abstract: Device miniaturization is an important part of VLSI design, which refers to reduction in dimension of device by keeping all other characteristic constant. As technology node is moving in submicron region, the performance of the device degrades due to short channel effects and narrow channel effects. The key issues due to these effects are drain-induced-barrier-lowering (DIBL), leakage current, hot electron reliability, punch through, sub-threshold slope, oxide breakdown, mobility, body effect, parasitic capacitance and parasitic resistance. In this paper, we have done in depth study of short channel effects. Then, we have provided their remedies by Substrate Engineering. The comparison of Ultra-thin bulk (UTB), Partially Depleted SOI MOSFET and Fully Depleted SOI MOSFET have been done by various performance parameters using Silvaco TCAD tool.

Keywords: Short and Narrow Channel Effects, Partially Depleted SOI MOSFET and Fully Depleted SOI MOSFET.

I. INTRODUCTION

In the early 1960's, the co-founder of Intel Corporation, Gordon Moore observed that the total number of transistors on an integrated circuits doubles every year. He predicted that this trend will be continued in future as shown in fig.1 [1]. In subsequent years, this scenario will move down a bit, but the density of data doubled approximately every 18 months, and thus Moore's defines this definition as the current definition. When the magnitude of the channel length is of the same order as that of the

width of depletion layer of source and drain junction, then the MOSFET devices is considered to be short.

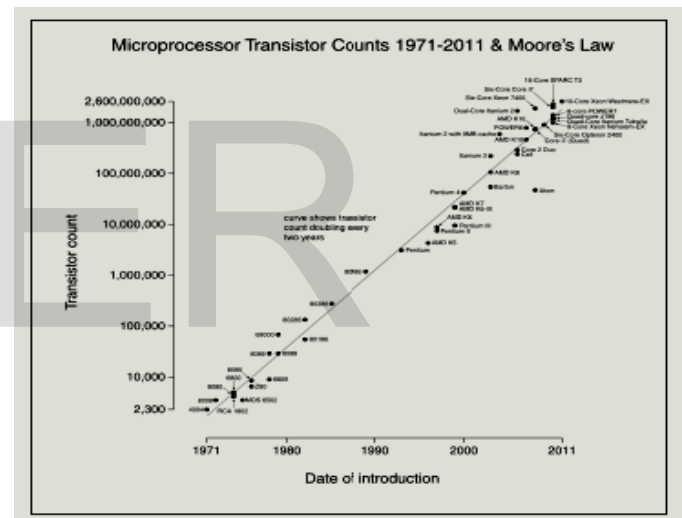


Fig.1: Plot of CPU Transistor Counts against Dates Of Introduction & Moore's Law.

In the MOSFET device if the length of the channel L is reduced upto certain extent, then the speed of the device increases and hence, the device will perform faster. Simultaneously the number of component per chip also increases. Due to reduction in the channel length of the device, the so called Short channel effects (SCE) arises. These effects are DIBL (Drain Induced Barrier Lowering), Punch Through, Hot Electron Reliability, Sub-threshold Current, Oxide Breakdown which severely affects MOS device performance.

In an order to reduce these effects Ultra-thin bulk (UTB), Partially Depleted SOI MOSFET and Fully Depleted SOI MOSFET [9] have been proposed. SOI reduces the above effects with least process complexities. SOI provides higher immunity to SCE (Leakage issues, sub-threshold and variability issues due to scaling) which further shrinks CMOS Technology. These devices are very attractive in terms of low power dissipation, higher speed VLSI applications because they have small parasitic capacitance and parasitic resistance. In general, it is believed that thin film SOI MOSFET's have ability to withstand SCE compared with bulk MOSFET's. In this paper, we have studied and compared the simulation results of Ultra-thin bulk (UTB), Partially Depleted SOI MOSFET and Fully Depleted SOI MOSFET [9] by various performance parameters using Silvaco TCAD tool.

II. SHORT CHANNEL EFFECT

Short channel effect (SCE) arises when the magnitude of channel length is of the same order as that of the width of depletion layer of source and drain junction. Due to these the device behaves differently from other MOSFET's. In MOSFET device, if the length of the channel length L is reduced upto certain extent, then the operation speed of the device increases and the number of components per chip also increases, then the so-called short-channel effects arise. These short channel effects are assigned to two physical phenomenons: the limitation enforced on electron drift characteristics in the channel and due to the shortening channel length the threshold voltage changes. In particular different short-channel effects can be drain induced barrier lowering (DIBL) [5], punch through, sub-threshold slope, hot electron reliability [8], leakage current [6] [7], oxide breakdown, mobility, body effect, impact ionization, velocity saturation, parasitic capacitance and resistance.

III. SUBSTRATE ENGINEERING

Due to scaling, the technological as well as the economical benefits in very-large-scale-integrated (VLSI) circuits decreases. Thus the alternative way to increase the performance and speed of MOSFET's is to use different channel materials such as germanium and strained silicon. It has been believed that almost

all of the performance benefit in CMOS implementations will derive from the n- MOSFET, p- MOSFET demonstrate enhanced hole mobility, but the enhancement has been done to degrade at high vertical field.

If the scaling has to be done upto the limits of the ultimate scalability, the device has to be such that the conducting channel is strictly under gate control and diffusion of the lateral field is minimized. By increasing substrate doping, the minimization have been accomplished. When there is a subsequent increase in substrate doping, the thickness of the depletion layer reduces under the channel and due to this strong coupling between the bulk and the channel is formed. This results in reduction of inversion charge density and weakens the gate control. If the thickness of oxide scaled down, there occurs strong coupling between the gate and the channel. With the thickness reduction of gate oxide the supply voltage also scaled down and thus there is a need to control threshold voltage more precisely. Due to dopant fluctuations, higher bulk doping leads to more variations in threshold voltage. Therefore there is a need to reduce doping concentration of bulk, which is incompatible with the requirement of strong bulk control. A method to minimize the effect of bulk doping concentration is to reduce the bulk material. A SOI MOSFET structure have limited amount of bulk material on an insulating substrate. Partially Depleted MOSFET's are used in a number of applications. With the advancement in the technology the thinning of silicon film give rise to fully depleted SOI MOSFETS.

IV. SILICON-ON-INSULATOR (SOI)

As devices are made smaller some effects severely affects the device. All silicon device structures have some built-in problems related with parasitic circuit elements which are arising from junction capacitance. A method to avoid these type of problems is to fabricate devices in small islands of silicon on an insulating substrate [2] with Silicon- On- Insulator (SOI) wafers. In SOI, transistors are formed in thin layers of silicon that are separated from the main body of the wafer by a layer of electrical insulator, usually silicon dioxide [9]. Fig.2 [2] given below presents comparison of bulk MOSFET structure and SOI MOSFET structure. The capacitance at the source and drain junctions can be significantly

reduced by SOI by removing the depletion regions extending into the substrate. The above technique helps in reducing the RC delay and hence provides a higher speed performance of SOI CMOS devices compared to bulk CMOS mainly at lower power supply voltage.

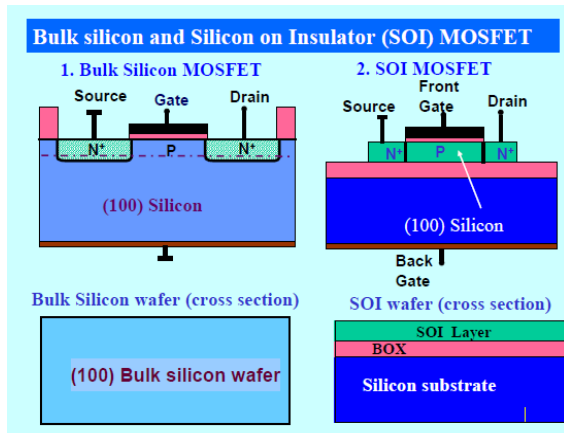


Fig.2: Comparison of Bulk MOSFET Structure and SOI MOSFET Structure.

The key advantages of using SOI are as, Reduced Source and Drain to Substrate Capacitance, Absence of Latch up, Lower Passive current, Higher Density and Low cost. SOI devices can be classified into two main categories: FDSOI (fully depleted SOI) MOSFETs and PDSOI (partially depleted SOI)

V. PARTIALLY DEPLETED SOI

In PD-SOI, the body is wider than the depletion region. As a result, variation in bulk voltage can occur depending on the amount of charge present. Because of the body effect [3] the variations in charge changes the V_t . IN PD-SOI as shown in fig.3 body is partially depleted and floats independent from bulk substrate. This floating body boosts performance but introduces history effect, kink effect.



Fig.3: Partially Depleted SOI Transistor

VI. FULLY DEPLETED SOI

Fully Depleted Silicon on Insulator or FD-SOI is a planar process technology. As shown in fig.4, an ultra-thin layer of insulator called the buried oxide is placed above the base silicon. This ultra thin bulk thickness can be 10 or 25nm. Finally, a very thin silicon film makes the transistor channel. Because of this thin silicon film, doping of the channel is not required, hence making the transistor Fully Depleted. Hence it is called “ultra-thin body and buried oxide Fully Depleted SOI” or UTBB-FD-SOI [10].

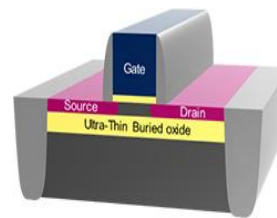


Fig. 4: Ultra-thin Body and Buried Oxide Fully Depleted SOI.

In terms of construction, this very thin silicon layer allows the silicon under the transistor gate, known as the body of the transistor, to be fully depleted of charges. This makes the gate to have a good control over the full transistor body. Hence making it better than a Bulk CMOS transistor, as supply voltage (hence gate voltage) decreases and transistor dimensions also reduces.



Fig.5: Fully Depleted SOI Transistor

FD-SOI helps in solving issues related to scaling, leakage and variability to further reduce CMOS technology beyond 28nm. It offers several advantages [4]. The superb electrostatic control of the transistor boosts the performance of FD-SOI and hence VDD gets lower (resulting low power consumption) at the same time creating an impressive performance. FD-SOI reduces the random fluctuation of dopant atoms, hence making transistor threshold (V_t) less variable. Because of this SRAM becomes

stable and dense, and functions at a very low VDDmin. FD-SOI is intrinsically Low Leakage and retrieves better control over Short Channel Effects. One consequence is that as we are able to shrink the gate length aggressively, devices gets fit into smaller and smaller pitches and hence increase logic density. These above attributes are outcomes of using Ultra-Thin Body devices, as they require no doping in channel (and consequently do not get affected from Random Dopant Fluctuation, which is becoming an crucial problem for Bulk CMOS) and exhibit wonderful electrostatic control of the channel. Therefore gets concluded into excellent VT variability, limited Short Channel Effects, low DIBL (Drain Induced Barrier Lowering), very good Sub-threshold Slope, and diode leakage and minimum junction capacitance [11], [12].

VII. COMPARATIVE STUDY

The analogy between Partially Depleted SOI and Fully Depleted SOI is shown below in table 1.

Table 1: Comparative Study Of PD-SOI and FD-SOI

| | Structural Differences | Target Applications | Advantages | Challenges |
|--------|---|---|---|---|
| PD-SOI | It has doped channel | High performance microprocessor | Well understood | Physical units are scalable to achieve high performance |
| | Thickness of top silicon 50-90 nm | Embedded, Analog, Automotive power, Aerospace | Industrially proven | |
| | Insulating box layer is 100 to 200 nm thick | | Easy to manufacture | |
| FD-SOI | It often uses undoped or lightly doped channel | High performance microprocessor | Leakage and power consumption are reduced | Very thin bodies are challengeable. |
| | Thickness of top silicon is 5 to 20 nm | Low power electronics | For undoped channels random fluctuations in V are minimized | |
| | Insulating box layer may also be Ultra thin(5-50nm) | Ultra low power devices | Easier to control SCE | |

VIII. CONCLUSION

SOI permits transistors that may succeed beyond the boundary of the standard CMOS technology. For SOI circuits a dedicated technology and design is needed to overcome the limitations of microelectronics. With the improvement in the quality of the material and better control over the technology, the processing of alternative devices becomes more practical. Hence concluded that SOI has wide applications in the world of Nanoelectronics. Our result shows that the thickness of SOI T_{Si} limits the scaling potential of FD to about 4 T_{Si} . The performances of Fully Depleted devices are better as compared to Partially Depleted devices. PD devices offer the advantage of improved sub threshold behavior at the shorter gate length at the cost of lower on-currents.

IX. FUTURE SCOPE

The MOSFET gate engineering has become progressively important technology component in the overall design of a transistor. Because of better scalability and immunity to short channel effects, devices such as double-gate (DM DG) MOSFETs, Tri-gate MOSFET, Flexfet and Finfet are being used now days for CMOS applications.

X. ACKNOWLEDGEMENT

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